REMARKS

Claims 6-25 and 27-40 are pending in this application. By this Amendment, the specification and claims 6-9, 11-12, 14-15, 17-19 and 25 are amended, new claims 27-40 are added and claims 1-5 and 26 are canceled without prejudice or disclaimer. Various amendments are made for clarity and are unrelated to issues of patentability.

The Office Action rejects claim 1 under 35 U.S.C. §112, second paragraph. By this Amendment, claim 1 is canceled. Thus the rejection is moot.

Applicants gratefully acknowledge the Office Action's indication that claims 21-24 contain allowable subject matter. See also dependent claims 30 and 39. However, as will be described below, all claims are believed to define patentable subject matter.

The Office Action rejects claims 1-2 and 5-8 under 35 U.S.C. §102(e) over U.S. Patent 6,467,004 to Iwamura et al. (hereafter Iwamura). The Office Action rejects claims 3-4 and 9-20 under 35 U.S.C. §103(a) over Iwamura and U.S. Patent 6,173,356 to Rao, U.S. Patent 5,867,683 to Witt et al. (hereafter Witt), U.S. Patent 6,505,269 to Potter, U.S. Patent Publication 2002/0156995 to Martin et al. (hereafter Martin), U.S. Patent Publication 2003/0037226 to Tsuruta et al. (hereafter Tsuruta), U.S. Patent 6,052,802 to Zahir et al. (hereafter Zahir), U.S. Patent 6,498,764 to Won et al. (hereafter Won), U.S. Patent 5,586,282 to Iino et al. (hereafter Iino), U.S. Patent Publication 2002/086589 to Makuta et al. (hereafter Makuta), Applicants' Admitted Prior Art (hereafter AAPA) and/or U.S. Patent Publication 2004/0199739 to Jeddeloh. The Office Action also rejects claims 25-26 under 35 U.S.C. §103(a) over U.S. Patent

6,732,247 to Berg et al. (hereafter Berg) and AAPA. The rejections are respectfully traversed with respect to the pending claims.

Independent claim 6 recites a plurality of systolic memory arrays each divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes.

In rejecting previous claims 5 and 6, the Office Action broadly cites Iwamura's Abstract and column 4, lines 12-14 and column 4, lines 33-46. These features merely relate to a pipelined device. However, Iwamura does not teach or suggest all the features of independent claim 6. More specifically, Iwamura does not relate to the claimed plurality of systolic memory arrays each divided into banks and each of the memory arrays arranged in a pipeline architecture.

Iwamura discloses different memory arrays that may be provided on a chip. See, for example, Figure 25. However, as is expressly described in Iwamura, a signal line 2560 supplies an address signal from the peripheral circuit 2550-1 to the address decoders 2520-12 to 2520-7. See column 1, lines 50-65. Figure 25 does not correspond to the features of independent claim 6. Additionally, the cited sections merely relate to a pipelined processing device and memory device. There is no discussion in Iwamura relating to a plurality of systolic memory arrays each divided into banks where each of the memory arrays is arranged in a pipeline architecture. Furthermore, there is no suggestion in Iwamura for the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes that interface with the

plurality of memory arrays. Iwamura therefore does not teach or suggest all the features of independent claim 1. Accordingly, independent claim 1 defines patentable subject matter.

Independent claim 35 recites a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion. For at least similar reasons as set forth above, Iwamura does not teach or suggest all the features of independent claim 35.

Furthermore, independent claim 25 recites the systolic memory including a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion. For at least similar reasons as set forth above, Iwamura does not teach or suggest all the features of independent claim 25. Thus, independent claim 25 defines patentable subject matter.

Accordingly, each of independent claims 6, 25 and 35 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

For example, dependent claim 31 recites a plurality of pipeline registers, each register to couple to one of the separate systolic memory arrays. Still further, dependent claim 32 recites each register is coupled to one end of a corresponding one of the systolic memory arrays. See

also dependent claims 36 and 37. The applied references do not teach or suggest these features. Thus, these dependent claims define patentable subject matter at least for this additional reason.

Furthermore, when addressing dependent claim 19, the Office Action (on page 14) asserts that the concept of a systolic memory array is described in applicant's own admitted prior art under the applicant's background section. The Office Action then cites Makuta col. 15, lines 65-67 and FIG. 7, item 50 as disclosing a peripheral circuit along one side of a memory array. However, Makuta does not include 15 pages. Therefore, applicants are uncertain of the cited features in Makuta. Still further, the Office Action references Figure 7, item 50 relating to the peripheral circuit. However, this does not relate to peripheral access for one systolic memory array being accomplished from one side of the one systolic memory array. Furthermore, contrary to the statements made in the Office Action, applicants' background section does not describe the concept of the systolic memory array. Rather, paragraph [3] of the present specification describes systolic structures. Furthermore, paragraphs [5] and [6] relate to embodiments of the present invention and therefore are not considered as prior art. Applicants respectfully submit that the rejections based applicants' background section is improper. Still further, Makuta's peripheral circuit does not provide the claimed features. For at least these reasons, dependent claim 19 defines patentable subject matter. Additionally, each of dependent claims 32-33 and 40 also defines patentable subject matter for at least similar reasons.

Still further, dependent claim 17 recites a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks of one of the systolic memory arrays one cycle at a time. The Office Action

states that Iwamura and Witt do not disclose these features. The Office Action then relies on Iino as disclosing the missing features. However, Iino may not merely be combined with Iwamura and Witt to obtain the clamed features. Stated differently, Iwamura may not be modified as alleged in the Office Action. Dependent claim 19 defines patentable subject matter at least for this additional reason.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 6-25 and 27-40 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

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Date: May 1, 2006